IN THE CLAIMS

1. (Previously Amended) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table; and

oxidizing the metal layer to form a metal oxide layer on the body region.

2. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

3. (Previously Canceled)

4. (Original) The method of claim 3, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

5. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

6. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

7. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

8. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

9. (Previously Amended) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table; and

oxidizing the metal layer using a krypton(Kr)/oxygen (O2) mixed plasma process to form a metal oxide layer on the body region.

10. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

11. (Previously Canceled)

D1 Cont.

12. (Original) The method of claim 11, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

13. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

14. (Previously Amended) A method of forming a transistor, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

15. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

16. (Previously Canceled)

17. (Original) The method of claim 16, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

18. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

19. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

D1 Cont.

20. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

21. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

22. (Previously Amended) A method of forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

23. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

24. (Previously Canceled)

25. (Original) The method of claim 24, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

26. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

D' Cont.

27. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

28. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

29. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

30. (Previously Amended) A method of forming an information handling system, comprising:

forming a processor;

forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

D1 Cont.

31. (Original) The method of claim 30, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

32. (Previously Canceled)

33. (Original) The method of claim 32, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

34. (Original) The method of claim 30, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

35. (Original) The method of claim 30, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

36. (Original) The method of claim 30, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

37. (Original) The method of claim 30, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

38. - 50. (Previously Withdrawn)

51. (Previously Amended) A transistor formed by the process, comprising:

forming a body region coupled between a first source/drain region and a second source/drain region;

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

52. (Original) The transistor of claim 51, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

D' cont.

53. (Previously Canceled)

54. (Original) The method of claim 51, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

55. (Previously Amended) A method of forming a gate oxide on a transistor body region, comprising:

electron beam evaporation depositing a zirconium layer on the body region; and

oxidizing the zirconium layer to form a metal oxide layer on the body region.

56. (Previously Amended) The method of claim 55, wherein oxidizing the zirconium layer includes oxidizing a zirconium layer to form an oxide with a conduction band offset in a range of approximately 5.16 eV to 7.8 eV.

57. - 61. (Previously Withdrawn)